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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/790,689	Applicant(s) ROO, PIERTE	
	Examiner Siu M. Lee	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 March 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-108 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-108 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 27, line 14, the reference number of phase controller should be 110 instead of 100.

Page 31, lines 8, 10, 12, recite the time delay element 205. Time delay element 205 should be changed to time delay element 310.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 5, 6, 8, 10, 14, 18, 19, 21, 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Lesea (US 6,946,870 B1).

(1) Regarding claims 1 and 14:

Lesea discloses a system comprising:

a plurality of information communication devices (configurable input/output block (IOB) 121-124, 131-134, 141-144, 151-154 in figure 1, column 2, lines 49-50); wherein

each of the plurality of information communication devices is responsive to a respective information communication clock signal (as discloses in figure 1, IOB 121-124 receives the CLK_0, IOB 131-134 receives the CLK_{90}, IOB 141-144 receives the CLK_{180}, IOB 151-154 receives the CLK_{270}, wherein each clock signal is separate by 90 degree in phase, column 3, lines 19-38, the IOBs are switched by the CLK signal); and

wherein each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal (as shown in figure 3, all the CLK0 to CLKN clock signal is associated with a common reference signal (CLK0), digital clock manager (DCM) 111 is configured to provide four output clock signals in response to an input clock signal CLK_{IN}, column 2, lines 60-63); and

wherein the phase controller ((digital clock manager (DCM) 111) is responsive to the common reference clock signal (digital clock manager (DCM) 111 is configured to provide four output clock signals in response to an input clock signal CLK_{IN}, column 2, lines 60-63);

wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

(2) Regarding claims 5 and 18:

Lesea discloses wherein the phase controller alters the phase of each information communication clock signal of each of the plurality of information

communication devices by a multiple of 90 degrees (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

(3) Regarding claims 6 and 19:

Lesea discloses wherein the phase of at least two of the information communication clock signal are substantially identical (input output blocks 122-124 receives clock signal that are substantially identical), and wherein a number of information communication clock signals with substantially identical phase (4 input output block receives a substantially identical clock) is less than a total number of information communication clock signal of the information communication system (4 identical information communication is less than a total of 16 information communication clock signal).

(4) Regarding claims 8 and 21:

Lesea discloses wherein the phase controller comprises a plurality of time delay elements (figure 3 discloses a detail of the digital clock manager 311 wherein the DCM 311 comprises a plurality of time delay element 315 and programmable delay lines 321, column 3, lines 62-67).

(5) Regarding claim 10 and 23:

Lesea discloses wherein the plurality of time delay elements are arranged in cascade (time delay elements 321 and 315 are arrange in cascade), and wherein each of the plurality of information communication devices is in communication with at least one of the plurality of time delay elements (each of the IOB 301 is in communication with at least one of the time delay element 321 and 315 as discloses in figure 3).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 8-18, 21-33, 36-40, 42-51, 53-62, 64, 91-94, 96-103, 105-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Lesea (US 6,946,870 B1).

(1) Regarding claims 1 and 14:

Cranford discloses a system comprising:

a plurality of information communication device (a plurality of transceivers (PHYs) 310 in figure 5, column 6, lines 24-25); wherein each of the of the plurality of information communication devices is responsive to a respective information communication clock signal (the phase control signal generated by the phase-lock loop circuit is applied to a string of delay circuits that produce a plurality of phased output control signals that are used to drive a plurality of transmitters, column 2, lines 51-54, each of the transceiver (PHYs) 310 is responsive to the phased control signal C11 to C1n, column 7, lines 14-16), and wherein each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal

(all the phased control signal is related to the reference clock signal 101 as shown in figure 5); and

a phase controller (phase control circuit 110 and a string of delay elements 120'), wherein the phase controller responsive to the common phase reference clock signal (output clock signal 103 of the phase control circuit 110, column 7, lines 2-3), and wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a known amount (the aspect of the invention can provide known, constant phasing between transceiver 310, column 6, lines 37-38, each information communication clock signal C11 to C1n is being delay by delay element D in 120', column 6, lines 31-39).

Cranford fails to disclose a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount.

However, Lesea discloses a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

It is desirable for a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to

employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(2) Regarding claims 2 and 15:

Cranford discloses wherein each of the plurality of information communication devices is responsive to the common reference clock signal altered by the phase controller (each of the transceiver (PHYs) 310 is responsive to the phased control signal C11 to C1n, column 7, lines 14-16), and wherein teach of the plurality of information communication devices comprises a device clock (clock generator circuit 510 in figure 5) for generating the respective information communication clock signal (C21 to C2m), using the common reference clock signal (the first plurality of phased clock signals C11 to C1n) are in turn provide to a plurality of clock generator circuits 510 that produce a second plurality of phased clock signal C21 to C2m, clock generator circuits 510 may implement a variety of clock processing functions, such as clock division to support multi-speed protocols, column 7, lines 10-13).

(3) Regarding claims 3 and 16:

Cranford discloses wherein the phase controller alters a phase of the common reference clock signal for each of the plurality of information communication devices by the predetermined amount to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (the multi-phase clock signal according to this aspect of the present invention can provide known, constant phasing between the transceiver 310, column 6, lines 36-39).

(4) Regarding claim 4, 17, 32, 39, 50, and 61:

Cranford discloses a reference clock signal generator for generating the common reference clock signal (a first phase control circuit 110 including a ring oscillator circuit 114 including a first string of delay circuits D that produce an output signal 103 that is phase locked to a reference clock signal 101 through the action of a loop control circuit 112 based on a comparison of the reference clock signal 101 and the output signal 103, column 4, line 65 – column 5, line 4).

(5) Regarding claims 5, 18, 33, 40, 51 and 62:

Lesea further discloses wherein the phase controller alters the phase of each information communication clock signal of each of the plurality of information communication device by a multiple of 90 degrees (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

(6) Regarding claims 6, 19, 35, 41, 52 and 63:

Lesea discloses wherein the phase of at least two of the information communication clock signal are substantially identical (input output blocks 122-124 receives clock signal that are substantially identical), and wherein a number of information communication clock signals with substantially identical phase (4 input output block receives a substantially identical clock) is less than a total number of information communication clock signal of the information communication system (4 identical information communication is less than a total of 16 information communication clock signal).

It is desirable wherein the phase of at least two of the information communication clock signal are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(7) Regarding claims 8, 21, 42 and 53:

Cranford discloses wherein the phase controller comprises a plurality of time delay elements (120' in figure 5 comprises a plurality of delay elements).

(8) Regarding claims 9, 22, 43 and 54:

Cranford discloses wherein the plurality of time delay elements comprises a plurality of delay locked loops (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops).

(9) Regarding claims 10, 23, 44, and 55:

Cranford discloses wherein the plurality of time delay elements are arranged in cascade (120' in figure 5 comprises a cascade of delay elements), and wherein each of

the plurality of information communication devices is in communication with at least one of the plurality of time delay elements (each of the transceivers (PHYs) 310 is connected to a first phased clock signals C11 to C1n produce by the delay element strings in 120' as shown in figure 5).

(10) Regarding claims 11, 24, 45, and 56:

Cranford discloses wherein the phase controller further comprises at least one delay locked loop (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops), wherein the at least one delay locked loop is in communication with each of the plurality of information communication devices via an information communication channel (each of the phased clock signal is communicated with its respective transceiver 310), and wherein each information communication channel includes at least one of the plurality of time delay elements (each of the phased clock signal would pass through at least one delay element (delay element in 114 and delay element in 120') of the phase controller).

(11) Regarding claims 12, 25, 46 and 57:

Cranford discloses wherein the information communication system comprises an Ethernet transceiver (fast Ethernet transceiver (FET), column 3, lines 36-39).

(12) Regarding claim 13, 26, 36, 47, 58 and 64:

Cranford discloses wherein the Ethernet transceiver is compliant with I.E.E.E. 802.3ab (a multiport fast Ethernet transceiver (FET) chip implementing a 100Tx(IEEE standard 802.3) class I or in class 2 repeater, column 2, lines 13-15).

(13) Regarding claim 27:

Cranford discloses a method comprising the steps of:

generating an information communication clock signal (phased output control signal 121 in figure 1) in each of the plurality of information communication devices (the phase control circuit 120 and component 130 in figure 1), wherein each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal (input control signal 103) (the second phase control circuit 120 are configured to receive input control signals 130 and operative to generate phased output control signals 121 that are phased dependent upon the applied phase control signal 113, column 4, lines 33-37); and altering a phase of each information communication clock signal for each of the plurality of information communication devices by a known amount (the second phase control circuit 120, controlled delays can be produces such that the phased output signals 121 are phased with respect to one another by time intervals that are on the order of nanoseconds, column 4, lines 56-60, these delay circuit can be used to generate precisely phased control signal for operating the components, column 2, lines 57-67 ,the multi-phase clock signal according to this aspect of the present invention can provide known, constant phasing between the transceiver 310, column 6, lines 36-39).

Cranford fails to disclose a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount.

However, Lesea discloses a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

It is desirable for a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(14) Regarding claim 28:

Cranford discloses the method further comprising the step of receiving the common reference clock signal in each of the plurality of information communication devices (as shown in figure 1, each phase control circuit 120 receives the input control signal 103).

(15) Regarding claim 29:

Cranford discloses wherein the method further comprising the step of generating each information communication clock signal for each of the plurality of information

communication devices using the common reference clock signal (the second phase control circuit 120 are configured to receive input control signals 130 and operative to generate phased output control signals 121 that are phased dependent upon the applied phase control signal 113, column 4, lines 33-37, the second phase control circuit 120, controlled delays can be produces such that the phased output signals 121 are phased with respect to one another by time intervals that are on the order of nanoseconds).

(16) Regarding claim 30:

Cranford discloses the step of altering the phase of the common reference clock signal for each of the plurality of information communication devices by the predetermined amount to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (figure 5 discloses another embodiment of that the common reference clock signal (103) is being phase shifted for each of the information communication devices (clock generating circuit 510 and PHY 310) by a known amount, such that each phase clock signal C11 to C1n have a known phase difference, thus makes each of the second phased clock signal C21 to C2m have the same known phase different between one another, column 7, lines 1-16).

(17) Regarding claim 31:

Cranford discloses the step of time delaying the common reference clock signal supplied to each of the plurality of information communication devices by the predetermined amount (a string of delay element D in 120' produce a first plurality of

phased clock signal C11 to C1n, each of the multi-phased clock signal can provide known, constant phasing between the PHYs 310, since the phase clock signals have a constant phase difference between each other, therefore, each of them is being time delay with the same amount relatively to each other, figure 5)

(18) Regarding claims 37 and 48:

Cranford discloses a system comprising:

a plurality of information communication devices (a plurality of transceivers (PHYs) 310 in figure 5, column 6, lines 24-25), wherein each of the plurality of information communication devices is responsive to a respective information communication clock signal (the phase control signal generated by the phase-lock loop circuit is applied to a string of delay circuits that produce a plurality of phased output control signals that are used to drive a plurality of transmitters, column 2, lines 51-54, each of the transceiver (PHYs) 310 is responsive to the phased control signal C11 to C1n, column 7, lines 14-16), wherein each of the plurality of information communication devices is responsive to a common reference clock signal (the phase control signal 103), wherein the information communication clock signal of each of the plurality of information communication devices is associated with the common reference clock signal (the phase control signal 103 is provided to a string of delay elements 120', producing a plurality of phased clock signal C11 to C1n (information communication signal), therefore, the information communication signal of each of the plurality of information communication devices is associated with the common reference clock signal 103); and

a phase controller (phase control circuit 110 and a string of delay elements 120'), wherein the phase controller is responsive to the common reference clock signal (the first phase control circuit 110 including ring oscillator circuit 114 including a first string of delay circuit D that produce an output signal 111 that is phase locked to a reference clock signal 101 through the action of a loop control circuit 112 based on a comparison of the reference clock signal 101 and the output signal 111, column 4, line 65 – column 5, line 4).

Cranford fails to disclose wherein the phase controller alters a phase of the common reference clock signal for each of the plurality of information communication devices by a predetermined amount to alter a phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount.

However, Lesea discloses wherein the phase controller alters a phase of the common reference clock signal for each of the plurality of information communication devices by a predetermined amount to alter a phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

It is desirable for a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it

would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(19) Regarding claims 38 and 49:

Cranford discloses wherein each of the plurality of information communication devices comprises a device clock for generating the respective information communication clock signal using the common reference clock signal altered by the phase controller (each transceiver 310 has a clock generator circuit 510 that may implement a variety of clock processing functions, such as clock division to support multi-speed protocols, column 7, lines 10-12, figure 5).

(20) Regarding claim 59:

Cranford discloses a method comprising the steps of:

receiving a common reference clock signal (the input clock signal 103 in figure 5 produced by the phase control circuit 110), wherein each of the plurality of information communication device is responsive to the common reference clock signal (the phase control signal generated by the phase-lock loop circuit is applied to a string of delay circuits that produce a plurality oh phased output control signal that are used to drive a plurality of transmitter, column 2, lines 54-54);

altering a phase of the common reference clock signal for each of the plurality of information communication devices by a known amount (a input clock signal 103 is provide to a string of delay element 120" producing a plurality of phased clock signal C11 to C1n, column 7, lines 1-3, the multi-phase clock signal C11 to C1n according to

this aspect of invention can provide known, constant phasing between the transceivers 310, column 6, lines 36-38); and

generating an information communication clock signal for each of the plurality of information communication devices using the respective phase-altered common reference clock signal (the first phased clock signals C11 to C1n are in turn provided to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signals C21 to C2m, column 7, lines 3-6).

Cranford fails to disclose the phase controller alters a phase of the common reference clock signal for each of the plurality of information communication devices by a predetermined amount to and wherein a phase of each information communication clock signal of each of the plurality of information communication devices is altered by the predetermined amount.

However, Lesea discloses a method wherein the phase controller alters a phase of the common reference clock signal for each of the plurality of information communication devices by a predetermined amount and wherein a phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

It is desirable for a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it

would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(21) Regarding claim 60:

Lesea further discloses time delaying the common reference clock signal supplied to each of the plurality of information communication devices by the predetermined amount (the delay element 321 in figure 3 delay the common reference clock signal CLK_0 supplied to each of the plurality of input output block 301 by the predetermined amount (90 degree), figure 3).

It is desirable to time delaying the common reference clock signal supplied to each of the plurality of information communication devices by the predetermined amount because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(22) Regarding claim 91 and 100:

Cranford discloses a system comprising:

a reference clock signal generator (phase control circuit 110) for generating a common reference clock signal (output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, column 7, lines 8-10);

a plurality of information communication devices (transceiver (PHYs) 310), wherein each of the plurality of information communication devices is responsive to the

common reference clock signal (the phase control signal generated by the phase-lock loop circuit is applied to a string of delay circuits that produce a plurality f phased output signals that are used to drive a plurality of transmitter, column 2, lines 51-54), wherein each of the plurality of information communication devices is responsive to a respective information communication clock signal (the first plurality of phased clock signal C11 to C1n are in turn provide to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signal C21 to C2m to drive the PHYs 310, column 7, lines 3-6), wherein each information communication clock signal of each of the plurality of information communication devices is associated with the common reference clock signal (the output signal 103 provided to a string of delay 120' to generate a first plurality of phased clock signal and then the first plurality of phased clock signal C11 to C1n are in turn provide to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signal C21 to C2m to drive the PHYs 310, therefore the each information communication clock signal of each of the plurality of information communication devices is associated with the common reference clock signal 103, column 7, lines 1-22); and

a phase controller (phase control circuit 110 and string of delay element 120'), wherein the phase controller is responsive to the common reference clock signal (delay element is operative to produced phased output control signals from at least one input control signal responsive to the phase control signal, column 2, lines 43-46), wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a known amount (a string

of delay elements D 120' produce phased clock signals C11 to C1n from an input clock signal 103responsive to phase control signal 113, the multi-phase clock signals C11 to C1n can provide known, constant phasing between the transceiver 310, column 6, lines 36-39), and

wherein each of the plurality of information communication devices comprises a device clock for generating the respective information communication clock signal using the common reference clock signal altered by the phase controller (the first plurality of phased clock signal C11 to C1n are in turn provide to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signal C21 to C2m to drive the PHYs 310, column 7, lines 3-6).

Cranford fails to disclose a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount.

However, Lesea discloses a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

It is desirable for a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to

employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(23) Regarding claims 92 and 101:

Lesea discloses in claim 91 and 100 that a phase controller alters a phase of the each information communication clock signal of each of the plurality of information communication devices by a predetermined amount.

Cranford discloses wherein the phase controller (phase control circuit 110 and 120' in figure 5) alters a phase of the common reference clock signal (the output signal 103 of phase control circuit 110) for each of the plurality of information communication devices (C11 to C1n are each different by a known amount of phase shift) by the known amount to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the known amount (the multi-phase clock signals C11 to C1n is use to drive the transceiver PHYs 310 and each of them is different by a known amount of phase shift, column 6, lines 36-39).

(24) Regarding claims 93 and 102:

Lesea further discloses wherein the phase controller alters the phase of each information communication clock signal of each of the plurality of information communication device by a multiple of 90 degrees (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

(25) Regarding claim 94 and 103:

Lesea discloses wherein the phase of at least two of the information communication clock signal are substantially identical (input output blocks 122-124

receives clock signal that are substantially identical), and wherein a number of information communication clock signals with substantially identical phase (4 input output block receives a substantially identical clock) is less than a total number of information communication clock signal of the information communication system (4 identical information communication is less than a total of 16 information communication clock signal).

It is desirable wherein the phase of at least two of the information communication clock signal are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(26) Regarding claims 96 and 105:

Cranford discloses wherein the phase controller comprises a plurality of time delay elements (a string of time delay elements D in 120' in figure 5, column 7, lines 1-2).

(27) Regarding claims 97 and 106:

Cranford discloses wherein the plurality of time delay elements comprises a plurality of delay locked loops (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase

control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops).

(28) Regarding claims 98 and 107:

Cranford discloses wherein the plurality of time delay elements are arranged in cascade (120' in figure 5 comprises a cascade of delay elements), and wherein each of the plurality of information communication devices is in communication with at least one of the plurality of time delay elements (each of the transceivers (PHYs) 310 is connected to a first phased clock signals C11 to C1n produce by the delay element strings in 120' as shown in figure 5).

(29) Regarding claims 99 and 108:

Cranford discloses wherein the phase controller further comprises at least one delay locked loop (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops), wherein the at least one delay locked loop is in communication with each of the plurality of information communication devices via an information communication channel (each of the phased clock signal is communicated with its respective transceiver 310), and wherein each information communication channel includes at

least one of the plurality of time delay elements (each of the phased clock signal would pass through at least one delay element (delay element in 114 and delay element in 120') of the phase controller).

6. Claims 65-70, 72-83, 85-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Lesea (US 6,946,870 B1) and Bishop et al. (US 2005/0135299 A1).

(1) Regarding claims 65 and 78:

Cranford discloses a transceiver comprises:

a plurality of information communication devices (a plurality of transceivers (PHYs) 310 in figure 5, column 6, lines 24-25), wherein each of the plurality of information communication devices is responsive to a respective information communication clock signal (the first plurality of phased clock signals C11 to C1n are in turn provided to a plurality of clock generating circuits 510 that produce a second plurality of phased clock signal C21 to C2m, column 7, lines 3-6, the phased clock signals are for driving the transmitter, column 2, lines 51-54), and wherein each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal (all the phased clock signal is associated with the output signal 103 of the phase control circuit 110, column 4, line 65 – column 5, lines 4); and

a phase controller (a string of delay elements 120'), wherein the phase controller is responsive to the common reference clock signal (the output signal of the phase

control circuit is delay by 120' and output a plurality of phased clock signal), and wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a known amount (these delay circuit can be used to generate precisely phased control signal for operating the components, column 2, lines 57-67 ,the multi-phase clock signal according to this aspect of the present invention can provide known, constant phasing between the transceiver 310, column 6, lines 36-39).

Cranford fails to (a) disclose the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount and (b) a plurality of transceivers.

With respect to (a), Lesea discloses a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

It is desirable for a phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

With respect to (b), Bishop et al. discloses a plurality of transceivers (plurality of remote transceiver 160 as shown in figure 1).

It is desirable to use a plurality of transceivers because it supports high speed access of information. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Bishop et al. in the system of Cranford and Lesea to improve the performance of the system.

(2) Regarding claim 66 and 79:

Cranford discloses wherein each of the plurality of information communication device is responsive to the common reference clock signal altered by the phase controller (the output signal of the phase control circuit is being phase delay by 102' and then provided to the plurality of clock generating circuit 510 to generate the phased clock signal C21 to C2m to drive the transceiver (PHYs) 310), and wherein each of the plurality of information communication devices comprises a device clock (clock generating circuit 510) for generating the respective information communication clock signal using the common reference clock signal altered by the phase controller (each transceiver 310 has a clock generator circuit 510 that may implement a variety of clock processing functions, such as clock division to support multi-speed protocols, column 7, lines 10-12, figure 5).

(3) Regarding claims 67 and 80:

Lesea discloses in claim 91 and 100 that a phase controller alters a phase of the each information communication clock signal of each of the plurality of information communication devices by a predetermined amount.

Cranford discloses wherein the phase controller (phase control circuit 110 and 120' in figure 5) alters a phase of the common reference clock signal (the output signal 103 of phase control circuit 110) for each of the plurality of information communication devices (C11 to C1n are each different by a known amount of phase shift) by the known amount to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the known amount (the multi-phase clock signals C11 to C1n is use to drive the transceiver PHYs 310 and each of them is different by a known amount of phase shift, column 6, lines 36-39).

(4) Regarding claim 68 and 81:

Cranford discloses a reference clock signal generator for generating the common reference clock signal (a first phase control circuit 110 including a ring oscillator circuit 114 including a first string of delay circuits D that produce an output signal 103 that is phase locked to a reference clock signal 101 through the action of a loop control circuit 112 based on a comparison of the reference clock signal 101 and the output signal 103, column 4, line 65 – column 5, line 4).

(5) Regarding claims 69 ad 82:

Lesea further discloses wherein the phase controller alters the phase of each information communication clock signal of each of the plurality of information communication device by a multiple of 90 degrees (each of the CLK_0, CLK_{90}, CLK_{180}, and CLK_{270} is different by 90 degree in phase, column 3, lines 1-18).

(6) Regarding claims 70 and 83:

Lesea discloses wherein the phase of at least two of the information communication clock signal are substantially identical (input output blocks 122-124 receives clock signal that are substantially identical), and wherein a number of information communication clock signals with substantially identical phase (4 input output block receives a substantially identical clock) is less than a total number of information communication clock signal of the information communication system (4 identical information communication is less than a total of 16 information communication clock signal).

It is desirable wherein the phase of at least two of the information communication clock signal are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system because it reducing the high transient current associated with simultaneous switched outputs (column 1, lines 22-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Lesea in the system of Cranford to improve the reliability of the system.

(7) Regarding claims 72 and 85:

Cranford discloses wherein the phase controller comprises a plurality of time delay elements (a string of time delay elements D in 120' in figure 5, column 7, lines 1-2).

(8) Regarding claims 73 and 86:

Cranford discloses wherein the plurality of time delay elements comprises a plurality of delay locked loops (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops).

(9) Regarding claims 74 and 87:

Cranford discloses wherein the plurality of time delay elements are arranged in cascade (120' in figure 5 comprises a cascade of delay elements), and wherein each of the plurality of information communication devices is in communication with at least one of the plurality of time delay elements (each of the transceivers (PHYs) 310 is connected to a first phased clock signals C11 to C1n produce by the delay element strings in 120' as shown in figure 5).

(10) Regarding claims 75 and 88:

Cranford discloses wherein the phase controller further comprises at least one delay locked loop (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops), wherein the at least one delay locked loop is in communication with each of the

plurality of information communication devices via an information communication channel (each of the phased clock signal is communicated with its respective transceiver 310), and wherein each information communication channel includes at least one of the plurality of time delay elements (each of the phased clock signal would pass through at least one delay element (delay element in 114 and delay element in 120') of the phase controller).

(11) Regarding claim 76 and 89:

Cranford discloses the number of plurality of transceiver equal to n+1.

Cranford is silent about the exact number of transceiver comprise one of four or eight. However, since n is a variable is there is no constrain on what n can be equal to, it would have been obvious that n can be equal to 3 or 7, thus make the number of transceiver equal to one of four or eight.

(12) Regarding claim 77 and 90:

Cranford discloses wherein each of the plurality of transceiver comprises an Ethernet transceiver (fast Ethernet transceiver (FET), column 3, lines 36-39).

7. Claims 4 and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Lesea (US 6,946,870 B1) in view of Watannabe et al. (US 2003/0197498 A1).

Lesea discloses all the subject matter as discussed in claim 1 except a reference clock signal generator for generating the common reference clock signal.

However, Watannabe et al. disclose a reference clock generator for generating the common reference clock signal (reference clock generator 10 generating the reference clock MCK, paragraph 3-5).

It is desirable to use a reference clock signal generator for generating the common reference clock signal because it provides a stable clock signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Watannabe et al. in the system of Lesea to increase the reliability of the system.

8. Claims 7, 20, 34, 95, 104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Lesea (US 6,946,870 B1) as applied to claims 1, 14, 27, 91, 100 above, and further in view of Ishikawa et al. (US 5,610,911).

Cranford discloses the phase controller comprises a phase locked loop (first phase control circuit 110 in figure 5, a first phase control circuit, e.g. a phase locked loop is operative to synchronize an output signal thereof through intermediate generation of a phase control signal, column 2, lines 39-43).

Cranford and Lesea disclose all the subject matter as discuss in claims 7, 20, 95, and 104 except a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of signal division of an output signal of the phase locked loop, wherein the output signal is associated with the information communication clock signal, and wherein the start time

of signal division of the output signal is varied to alter the phase of each information communication clock signal of each of the plurality of information communication devices.

However, Iskikawa et al. discloses the using of a sync signal phase control 14 in figure 3 to control the resetting time of the frequency divider 13 in order to change the phase of the output signal of the frequency divider (column 5, lines 55-column 6, 24, column 13, lines 4-7, 26-37, column 16, lines 20-31).

It is desirable to use a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of signal division of an output signal of the phase locked loop and wherein the start time of signal division of the output signal is varied to alter the phase of each information communication clock signal of each of the plurality of information communication devices because it provides a simple circuit for generating a plurality of phased clock signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to combine the PLL of Cranford with the sync signal phase control 14 and frequency divider 13 of Iskikawa et al. to generate a plurality of phased clock signal for each of he plurality of information communication devices so as to reduce the complexity of the system.

9. Claims 71 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Lesea (US 6,946,870

B1) and Bishop et al. (US 2005/0135299 A1) as applied to claims 65 and 78 above, and further in view of Ishikawa et al. (US 5,610,911).

Cranford discloses the phase controller comprises a phase locked loop (first phase control circuit 110 in figure 5, a first phase control circuit, e.g. a phase locked loop is operative to synchronize an output signal thereof through intermediate generation of a phase control signal, column 2, lines 39-43).

Cranford and Lesea disclose all the subject matter as discuss in claims 7, 20, 95, and 104 except a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of signal division of an output signal of the phase locked loop, wherein the output signal is associated with the information communication clock signal, and wherein the start time of signal division of the output signal is varied to alter the phase of each information communication clock signal of each of the plurality of information communication devices.

However, Iskikawa et al. discloses the using of a sync signal phase control 14 in figure 3 to control the resetting time of the frequency divider 13 in order to change the phase of the output signal of the frequency divider (column 5, lines 55-column 6, 24, column 13, lines 4-7, 26-37, column 16, lines 20-31).

It is desirable to use a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of signal division of an output signal of the phase locked loop and wherein the start time of signal division of the output signal is varied to alter the phase of each information

communication clock signal of each of the plurality of information communication devices because it provides a simple circuit for generating a plurality of phased clock signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to combine the PLL of Cranford with the sync signal phase control 14 and frequency divider 13 of Iskikawa et al. to generate a plurality of phased clock signal for each of he plurality of information communication devices so as to reduce the complexity of the system.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sterne et al. (US 5,818,839) discloses a timing reference for scheduling data traffic on multiple ports. Kohdaka (US 6,046,607) discloses logic circuit controlled by a plurality of clock signals. Wallace, Jr. et al. (US 6,346,100 B1) discloses ground bounce reduction technique using phased output and package de-skewing for synchronous buses.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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